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ANTICIPATED CARRY-MAJORITY LOGIC MODE

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-63-157

April 1963

R. A. Knoebel

Prepared for

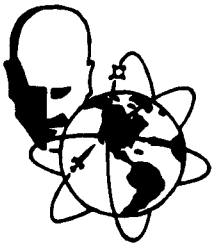
DIRECTORATE OF SYSTEM DESIGN

ELECTRONIC SYSTEMS DIVISION

AIR FORCE SYSTEMS COMMAND

UNITED STATES AIR FORCE

L. G. Hanscom Field, Bedford, Massachusetts



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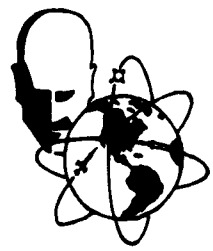

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ABSTRACT

The use of the majority (2 out of 3) logic element in anticipated carries for adders, multipliers, etc., yields very fast designs with only a moderate number of gates. The general theory of such carries is presented. This is applied to the design of a 48 bit adder. 164 majority gates give carries for all 48 bits with a maximum of 6 stages of delay. The relationship between delay and quantity of gates required is plotted.

INTRODUCTION

For generality let us assume we have two registers, A_n ($n \geq 1$) and B_n ($n \geq 1$), of indefinite length and an initial carry C_1. Let the carry to be summed with the nth stage be designated by C_n. All logic elements considered are two-out-of-three majority gates and are denoted by $\overset{2}{3} X_1X_2X_3$, i.e., $\overset{2}{3} X_1X_2X_3 = 1$ iff at least two of the X_i are 1.

The carry for one stage can be simply given as

1) $$C_{n+1} = \overset{2}{3}\ A_nB_nC_n$$

For two stages we can cascade:

2) $$C_{n+2} = \overset{2}{3}\ A_{n+1}\ B_{n+1}\ \overset{2}{3}\ A_nB_nC_n$$

For three stages we could cascade again but it is possible to eliminate one stage of delay (at the expense of one more gate) by applying the identity:

3) $$\overset{2}{3}\ V\ W\ \overset{2}{3}\ X\ Y\ Z = \overset{2}{3}\ \overset{2}{3}\ V\ W\ X\ \overset{2}{3}\ V\ W\ Y\ Z$$

Thus we obtain:

4) $$C_{n+3} = \overset{2}{3}\ A_{n+2}\ B_{n+2}\ \overset{2}{3}\ A_{n+1}\ B_{n+1}\ \overset{2}{3}\ A_n\ B_n\ C_n$$

5) $$= \overset{2}{3}\ \overset{2}{3}\ A_{n+2}\ B_{n+2}\ A_{n+1}\ \overset{2}{3}\ A_{n+2}\ B_{n+2}\ B_{n+1}\ \overset{2}{3}\ A_n\ B_n\ C_n$$

Notice that the last gate in 5) is simply C_{n+1} as given in 1) which, in applications, we probably would already have. Three stages of anticipation seems to be the maximum that we can obtain with only two stages of delay. For three stages of delay the maximum appears to be seven:

6) $$C_{n+7} = \overset{2}{3}\overset{2}{3}\overset{2}{3} A_{n+6} B_{n+6} A_{n+5} \overset{2}{3} A_{n+6} B_{n+6} B_{n+5} \overset{2}{3} A_{n+4} B_{n+4} A_{n+3}$$

$$\overset{2}{3}\overset{2}{3} A_{n+6} B_{n+6} A_{n+5} \overset{2}{3} A_{n+6} B_{n+6} B_{n+5} \overset{2}{3} A_{n+4} B_{n+4} B_{n+3}$$

$$\overset{2}{3}\overset{2}{3} A_{n+2} B_{n+2} A_{n+1} \overset{2}{3} A_{n+2} B_{n+2} B_{n+1} \overset{2}{3} A_{n} B_{n} C_{n}$$

Note again that the last line is C_{n+3} and note that two of the gates are repeated, viz: $\overset{2}{3} A_{n+6} B_{n+6} A_{n+5}$ and $\overset{2}{3} A_{n+6} B_{n+6} B_{n+5}$

GENERAL THEORY

To continue further without endless notation we take recourse to definition by induction. Also this will allow us to prove rigorously that we do indeed have a formula for anticipated carry by means of majority elements.

Definition:

7a) $$c(1, 1, n+1) = A_n \qquad (n \geq 1)$$

$$c(2, 1, n+1) = B_n \qquad (n \geq 1)$$

$$c(3, 1, n) = C_n \qquad (n \geq 1)$$

7b) $$c\ (i,j+1,n+j+1) = \overset{2}{3} A_{n+j} B_{n+j}\ c(i,j,n+j)$$

$$(i = 1,2,;\ j \geq 1;\ n \geq 1 \text{ or}$$

$$i = 3;\ j \geq 1;\ n \geq 0)$$

Note that in 7b) with i = 3 we obtain the cascaded carry for j+1 stages.

Proposition $c\ (i,j+k,n+j+k) = \overset{2}{3} c(1,k,n+j+k)\ c(2,k,n+j+k)\ c(i,j,n+j)$

8) $(i = 1,2,;\ j \geq 1;\ k \geq 1;\ n \geq 1$ or

$i = 3;\ j \geq 1;\ k \geq 1;\ n \geq 0)$

Proof (by induction on k). For k = 1, 8) is 7b) with substitution given by 7a). Assume the proposition is true for k. We shall prove it true for k+1.

$$c(i,j+k+1,n+j+k+1)$$

$$= \frac{2}{3} A_{n+j+k} B_{n+j+k} c(i,j+k,n+j+k) \qquad \text{(by 7b)}$$

$$= \frac{2}{3} A_{n+j+k} B_{n+j+k} \frac{2}{3} c(1,k,n+j+k)\, c(2,k,n+j+k)\, c(i,j,n+j) \qquad \text{(by ind. hyp.)}$$

$$= \frac{2}{3}\frac{2}{3} A_{n+j+k} B_{n+j+k} c(1,k,n+j+k)$$

$$\frac{2}{3} A_{n+j+k} B_{n+j+k} c(2,k,n+j+k)$$

$$c(i,j,n+j) \qquad \text{(by 3)}$$

$$= \frac{2}{3} c(1,k+1,n+j+k+1)\, c(2,k+1,n+j+k+1)\, c(i,j,n+j) \qquad \text{(by 7b)}$$

q.e.d.

The following corollary demonstrates the relationship between this proposition and anticipated carry.

Corollary $c(i,2^{m+1},\ n+2^{m+1})$

$$= \frac{2}{3} c(1,2^{m},\ n+2^{m+1})\, c(2,2^{m},\ n+2^{m+1})\, c(i,2^{m},\ n+2^{m})$$

Proof In 8) let $j=k=2^{m}$. $(i=1,2;\ m \geq 0;\ n \geq 1$ or

$i=3;\ m \geq 0;\ n \geq 0)$

We can form $c(i,2,n+2)$ from A_{n+1}, B_{n+1}, C_{n+1}, A_n, B_n. In turn we can obtain $c(i,2^2, n+^2)$ from $c(i,2,n+k)$ with $k=2,4$ and A_{n+1}, B_{n+1}. Continuing in this manner it is possible to build up a $2^m - 1$ stage anticipated carry with only m stages of delays. By a more sophisticated use of the proposition we can obtain all carries with little delay. In fact a k stage anticipated carry can always be designed with no more than $\log_2(k+1)$ stages of delay. This will all become clearer when we turn to a specific example.

By definition $c(3,j,n+j)$ is the carry to the jth stage calculated from the nth. Is there also a simple interpretation of $c(1,j,n+j)$ and $c(2,j,n+j)$? To answer this question consider what we mean by $c(3,j,n+j)$. We understand that $c(3,j,n+j) = 1$ if the sum of $A_{n+j-1}\ A_{n+j-2}\ldots\ A_n$*, $B_{n+j-1}\ B_{n+j-2}\ldots\ B_{n+j}$ and C_n is greater than or equal to 2^j. Equally simple is the interpretation of $c(1,j,n+j)$ and $c(2,j,n+j)$. $c(1,j,n+j) = 1$ iff the sum of $A_{n+j=1}\ A_{n+j-2}\ldots\ A_{n+1}\ A_n$ and $B_{n+j-1}\ B_{n+j-2}\ldots\ B_{n+1}$ is greater than or equal to 2^j-1 and $c(2,j,n+j) = 1$ iff the sum of $A_{n+j-1}\ A_{n+j-2}\ldots\ A_{n+1}\ 0$ and $B_{n+j-1}\ B_{n+j-2}\ldots\ B_{n+1}\ B_n$ is greater than or equal to 2^j-1 (the proof of these facts is tedious and is omitted).

H. Enderton has pointed out that addition with the majority element and its complement $\frac{2}{3}$ fits very well with the carry.

That is, $S_n = A_n \oplus B_n \oplus C_n$

$$= \tfrac{2}{3} A'_n\ \tfrac{2}{3} A_n B_n C_n\ \tfrac{2}{3} A'_n\ B_n\ C_n$$

$$= \tfrac{2}{3} A'_n\ C_{n+1}\ \tfrac{2}{3} A'_n\ B_n\ C_n$$

*By this is meant the binary number formed by replacing the A_j by their values, i.e., $\sum_{j=0}^{2^{i-1}} A_{n+j}\ 2^j$.

and $S'_n = {}^{2}_{3} A'_n C_{n+1}\ {}^{2}_{3} A'_n B_n C_n$

Thus for each stage of addition three gates are required.

APPLICATION

We now turn to the design of the carry system for a 48 bit adder. Since c(3,n,n) is the carry to the nth stage calculated from the first stage we set $C_n = c(3,n,n)$. We form the carries C_2, C_4, C_8, C_{16}, C_{32} as suggested by the corollary. To form the other carries C_n we look at the binary expansion of n and note the position k of the least significant one. Then $C_n = {}^{2}_{3} c(1,2^{k-1}, n)\ c(2,2^{k-1},n)\ C_{n-2^{k-1}}$. For example, if $n = 21_{10} = 10101_2$ then C_{21} propagates from C_{20}, which in turn propagates from C_{16}, which in turn propagates from C_8, etc. This procedure appears to yield an efficient design. Figure 1 illustrates this method.

For most $n \leq 32$, C_n will have a delay no greater than six stages. For the other $n \leq 32$ a simple modification of the gates reduces the delay to the maximum allowable. For $n > 32$ the problem is to build up the c(1,j,k) and c(2,j,k) efficiently in five stages of delay so that when gated with C_{32} the C_n will be formed. The method of obtaining a reasonably minimal solution is complicated and the reader is simply referred to Figure 2.

COMPARISON OF VARIOUS DESIGNS

Since 48 outputs are required for a complete carry system and since by a simple cascading we obtain all carries with 48 gates we have a minimal design. The delay is 48 stages. In the preceeding section we

achieved a carry system with six stages of delay and 164 gates. What happens in between these two extremes? Table 1 is a tabulation of delay vs. number of gates required. Figure 3 is a plot of this information. It is emphasized that in general it is not known if these designs are minimal.

Robert A. Knoebel/NSZ

Robert A. Knoebel

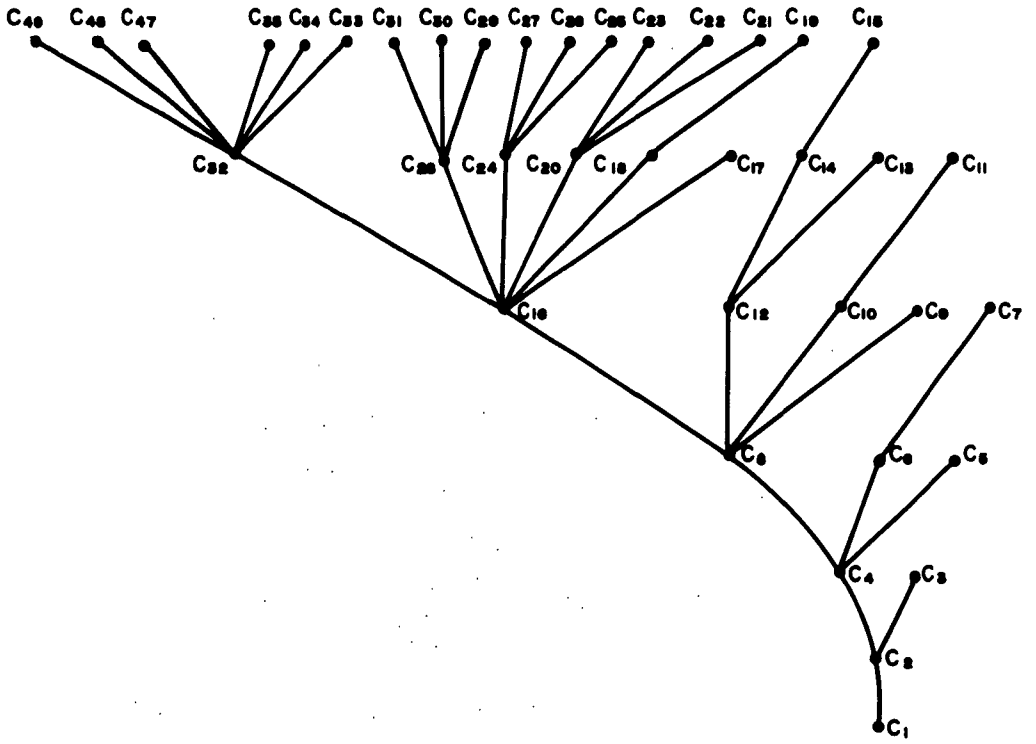

FIG. 1

DERIVATION OF CARRIES—EACH CARRY PROPAGATES INTO THOSE CARRIES WHICH SPROUT FROM IT.

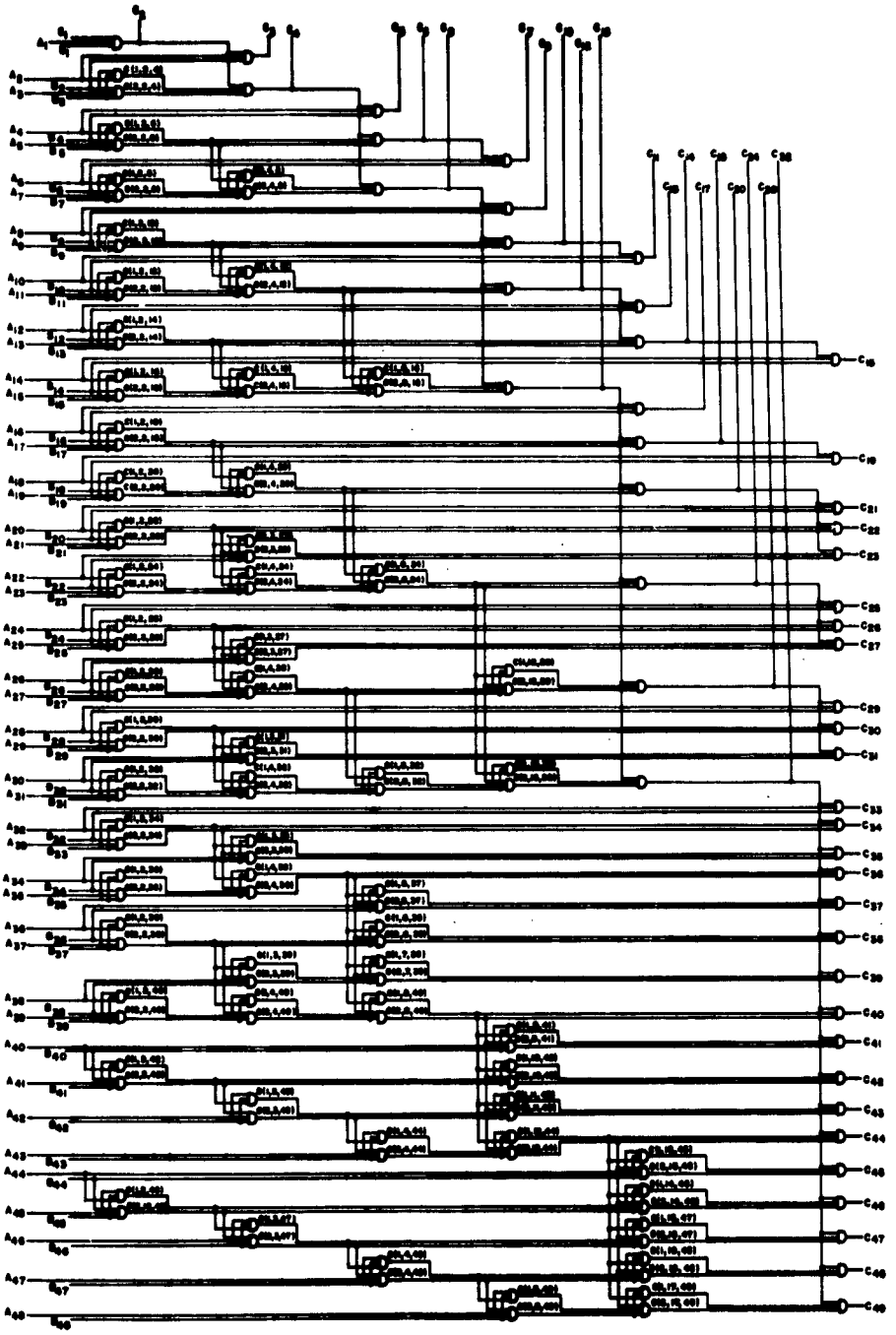

FIG. 2

ANTICIPATED CARRY WITH MAJORITY LOGIC. ALL CARRIES C_{2i} REQUIRED FOR THE ADDITION OF TWO 40 BIT REGISTERS ($A_{2i}, B_{2i}; 1 \leq i \leq 40$) AND AN INITIAL CARRY C_1 ARE GENERATED WITH 104 MAJORITY (5 OUT OF 31 GATES IN 6 STAGES OF DELAY. THERE IS CONSIDERABLE LOADING ON THE GATE GIVING C_{80}. IF A REASONABLE OUTPUT LOADING IS ASSUMED, SAY 6, THEN 3 MORE GATES ARE REQUIRED FOR A TOTAL OF 107 GATES. THE $c(i,j,k)$ ARE INTERMEDIATE SIGNALS WHOSE FUNCTION IS EXPLAINED IN THE TEXT.

NO. OF STAGES OF DELAY	6	7	8	9	14	21	22	32	48
NO. OF GATES	164	140	132	130	116	102	100	80	48

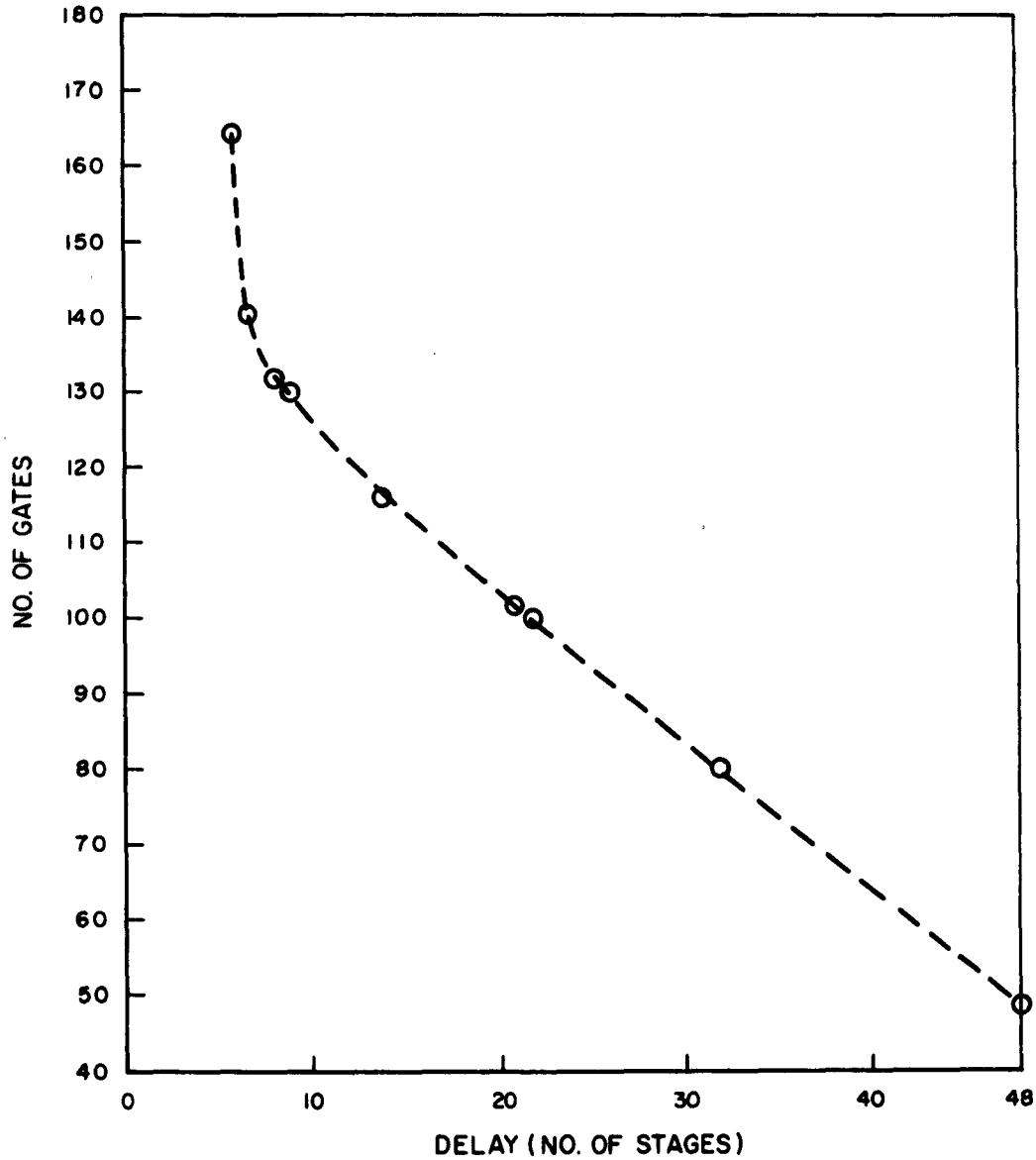

TABLE I

FIG. 3

COST vs. DELAY

FOR SELECTED DELAYS THE NUMBER OF GATES REQUIRED IN REASONABLY MINIMAL DESIGNS ARE TABULATED (PLOTTED)

IA-9754

Hq. ESD, L.G. Hanscom Field, Bedford, Mass.
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